Technicon AN 02-2025: Parallel connection of IGBT

REV.04, July 2025

General considerations

Parallel connection of IGBTs is used to increase total power of converter if the performance of single element is insufficient. This starts at the microscopic level with several 100.000 individual IGBT cells, then further in module by parallel connection of the chips and continues at circuit level by parallel connection of modules and entire inverter units.

Parallel connection of single switches allows covering wide power range with minimum nomenclature of power modules. Optimal utilization of parallel power switch units is achieved only with ideal static (i.e. during conduction period) and dynamic (i.e. during switching cycle) symmetry of currents in parallel nets. Main factors affecting the parallel use of IGBT is shown in Table 1.

Table 1. Factors influencing symmetrical current sharing

	Semiconductor		Module		Driver			Driver circuit			
	Saturation voltage $V_{CEsat}=f(i_C,V_{GE},T_j)$ $V_F=f(i_F,T_j)$	Transfer characteristics $I_C=f(V_{GE},T_j)g_{fs}$ $V_{GE(th)}$	Internal gate resistors $i_C=f(V_{GE}(t))$	Stray inductance of the commutation circuit L_σ	Jitter	Cycle time	Gate voltage (supply) $i_C=f(V_{GE}(t))$	Stray inductance Gate $L_{\sigma G}\,i_C=f(V_{GE}(t))$	Stray inductance Emitter $L_{\sigma E}\,i_C=f(V_{GE}(t))$	Gate resistors $i_C=f(V_{GE}(t))$	Emitter coupling, with shared emitter path
Static	x						x				
Dynamic		x	x	x	x	x	x	x	x	**x**	x

The following content will not discuss the circuit design: requirements for inverter with parallel switches (symmetric design of power DC and AC buses and control circuits) - is the responsibility of system designer. The Application Notes consider semiconductor parameters only to explain the IGBT performance in parallel operation.

Static current distribution

We assume that when using the concept of a central driver [1], the main current imbalance is determined by tolerance of static parameters: saturation voltage $V_{CE(sat)}$, gate threshold voltage $V_{GE(th)}$, diode forward voltage V_F.

The use of separate precision gate resistors R_{G_on}, R_{G_off} minimizes the effect of $V_{GE(th)}$ tolerance.
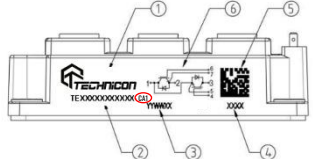
Due to the positive temperature coefficient (PTC) of $V_{CE(sat)}$, the static balance of currents in parallel IGBTs is provided automatically. However to minimize temperature difference between parallel IGBT it is desirable that tolerance in parallel IGBTs does not exceed 5%. Due to this we recommend to use in parallel IGBTs **with the same data-code**, produced under similar production conditions.

The most effect on current unbalance in parallel IGBTs is exerted by diode forward voltage V_F having a negative temperature coefficient in the range of operating currents. In cases where V_F deviation is critical for the application, IGBT modules should be selected according to V_F tolerance. **Only selected modules with the same V_F group can be connected in parallel, see recommendations below.**

Recommendations

For applications that require parallel connection of IGBT we give the following solutions.

1. To reduce temperature gradient between parallel IGBTs we recommend to use IGBTs **with the same data-code**. Position and format of the data-code is shown in Fig. 1. - IGBT marking specification (p.3).

Example	No.	Content
	1	Company Logo
	2	Type designation
	3	**Datacode: 6 digits YYWWL (YearYearWeekWeek 4 digits) +XX (lot number in 2 digits)**
	4	Product serial number in one sublot (4digits)
	5	QR
	6	Circuit diagram

Fig. 1. IGBT marking specification

2. For IGBT modules with the same lot number we conduct V_F monitoring and select IGBTs into different BIN groups to ensure V_F tolerance of one group within necessary limits. BIN group will be marked on the outer packaging and module case as shown in Fig. 2

Fig. 2. IGBT C2 case with BIN A1 group marking

Sample: V_F tolerance of BIN groups of IGBT TE450GB12C5R7 is shown in Table 2.

No.	Parameter		Conditions	Value			BIN
				Min	Max	Unit	
1	V_{F-U}	Upper FWD	$V_{GE}=0V$, $I_F=450A$	1,80	2,00	V	1
2	V_{F-L}	Lower FWD	$V_{GE}=0V$, $I_F=450A$	1,80	2,00	V	1
3	V_{F-U}	Upper FWD	$V_{GE}=0V$, $I_F=450A$	1,80	2,00	V	2
4	V_{F-L}	Lower FWD	$V_{GE}=0V$, $I_F=450A$	2,00	2,20	V	1

Summary

In order to minimize the influence of semiconductor properties on current distribution modules with the same data-code and the same V_F group (BIN code) should be connected in parallel. Possible current asymmetry must be taken into account for thermal calculations and definition of nominal current derating factor.

As a matter of fact, parallel use of power modules also needs to consider a lot of factors, first of all, the design of the power stage which is responsibility of customer. This document aims to tell customers how to use Technicon IGBTs in parallel to minimize current imbalance. Other influencing factors are not discussed there.

Reference

1. Niklas Hofstotter, Joachim Lamp. IGBT modules in parallel operation with central and individual driver board. SEMIKRON AN 17-001

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